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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/600,724 | 06/20/2003 | Sang-Don Yi | SAM-0422 | 5836 |

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| EXAMINER | |
|---|---|
| MAI, ANH D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 08/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/600,724 | YI, SANG-DON | |
| | Examiner | Art Unit | |
| | Anh D. Mai | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *1-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Group II, claims 7-27 in the reply filed on July 29, 2004 is acknowledged.

### *Claim Objections*

2. Claims 17 is objected to because of the following informalities:

Claim 17 recites: the method of claim 16, wherein the N-type impurities...

However, the "N-type impurities" neither exists in claim 16 nor claim 8.

The best way to correct this matter is to change claim 16 so that it depends on claim 15.

For the above reason, claims 16-17 will be determined as suggested.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 7, 13, 14 and 21-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Sun (U.S. Patent No. 5,496,764).

With respect to claim 7, Sun teaches a method of manufacturing an SOI wafer as claimed including:

a) forming an isolation insulating film (41) on a front face of a first semiconductor wafer (20) to define an active region and forming a bonding insulating film (11) on a front face of a second semiconductor wafer (10);

b) performing an ion implantation process so as to form a P-well and an N-well in the active region; (see col. 4, ll. 32-44);

c) pre-bonding the respective front faces of the first semiconductor wafer (20) and the second semiconductor wafer (10);

d) heating the bonded first (20) and second (10) semiconductor wafers at a predetermined temperature to completely bond the first (20) and second (10) semiconductor wafers with each other; and

e) polishing a back face of the first semiconductor wafer (20) to a bottom level of the isolation insulating film (41). (See Figs. 1-8, col. 2, line 5-col. 5, line 40).

Regarding the step c) pre-bonding, since the two wafers must be brought together prior to the heating, thus, step c) is met.

With respect to claim 13, in step a), the bonding insulating film (61) of Sun is a silicon oxide film.

With respect to claim 14, the bonding insulating film (31) of Sun is formed by thermally oxidizing the substrate silicon of the second semiconductor wafer (20).

With respect to claim 21, step d), heating the pre-bonded semiconductor wafers, of Sun is performed at a temperature (1000-1200 °C), thus, higher than a temperature at which ions implanted in the N-well and the P-well form a well.

Note that the temperature at which the ions implantation normally taken place are known to be below 1000 °C.

With respect to claim 22, step e) polishing, of Sun includes: preparing a back face of the first semiconductor wafer (20) to be a polishing face; and polishing substrate silicon on the back face of the first semiconductor wafer (20) using a polishing process. (See Fig. 8).

With respect to claim 23, polishing the substrate silicon of Sun includes grinding the back face of the first semiconductor wafer (20) using a grinder. This is the well known CMP.

With respect to claim 24, chemical mechanical polishing (CMP) of Sun is used as the polishing process.

With respect to claim 25, in the polishing process of Sun, the isolation insulating film (41) is used as a polishing stopper.

With respect to claim 26, after step e), the method of Sun further includes forming a protection insulating film (92) on a top surface of a semiconductor substrate. (See Fig. 9).

With respect to claim 27, the protection film (92) of Sun silicon oxide film.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun '764 as applied to claim 7 above, and further in view of Moore et al., (U.S. Patent No. 6,051,480).

With respect to claim 8, Sun teaches forming the isolation insulating film (41) on the front face of the first semiconductor wafer (20) including:

forming an isolation trench (31) on the semiconductor wafer (20);

forming a trench fill insulating film (41) so as to bury the isolation trench (31); and

planarizing the trench fill insulating film (41) using a planarization process. (See Figs. 3-5).

Thus, Sun is shown to teach all the features of the claim with the exception of explicitly disclosing formation of the mask insulating film.

However, Moore teaches the formation of an isolation insulating film (60) including:

forming a mask insulating film (20/30) on the surface of the first semiconductor wafer (10);

forming an isolation trench (40) on the mask insulating film (20/30) and the first semiconductor wafer (10);

forming a trench fill insulating film (60) so as to bury the isolation trench; and

planarizing the trench fill insulating film to a level of the mask insulating film using a planarization process. (See Figs. 1A-F).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the isolation trench of Sun to include the formation of a mask insulating film as taught by Moore to define the isolation areas and protect the surface of the semiconductor wafer. This is well known in the art.

With respect to claim 9, the mask insulating film of Moore includes a silicon oxide film (20).

With respect to claim 10, the mask insulating film of Moore further includes a silicon nitride film (30).

With respect to claim 11, the trench fill insulating film of Sun and Moore is a silicon oxide film.

With respect to claim 12, the planarization process of Sun and Moore includes chemical mechanical polishing (CMP).

5. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun '764 as applied to claim 7 above, and further in view of Ema et al., (U.S. Patent No. 5,789,788).

With respect to claim 15, Sun teaches step b) including: performing an ion implantation process so as to form a P-well and an N-well in the active region.

Thus, Sun is shown to teach all the features of the claim with the exception of disclosing the details of the well known ion implantation process.

However, Ema teaches an ion implantation process well known in the art to form the wells including:

However, Ema teaches an ion implantation process well known in the art to form the wells including:

forming a photoresist having a pattern (53) with which a region in which an N-well (12) is to be formed is opened, on the first semiconductor wafer (11);

implanting N-type impurities in the substrate silicon of the first semiconductor wafer (11) using ion implantation and using the patterned photoresist as (53) a mask; and

removing the photoresist (53). (See Fig. 3B).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the N-well of Sun using the well known ion implantation process as taught by Ema to form the N-well in the first semiconductor wafer.

With respect to claim 16, Sun teaches step b) including: performing an ion implantation process so as to form a P-well and an N-well in the active region.

Thus, Sun is shown to teach all the features of the claim with the exception of disclosing the details of the well known ion implantation process.

However, Ema teaches an ion implantation process well known in the art to form the wells including:

forming a photoresist having a pattern (54) with which a region in which an P-well (14) is to be formed is opened, on the first semiconductor wafer (11);

implanting P-type impurities in the substrate silicon of the first semiconductor wafer (11) using ion implantation and using the patterned photoresist as (54) a mask; and

removing the photoresist (54). (See Fig. 3C).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the P-well of Sun using the well known ion implantation process as taught by Ema to form the P-well in the first semiconductor wafer.

With respect to claim 17, the N-type impurities of Ema are well known 5-valence electron ions, including phosphorus (P).

With respect to claim 18, the P-type impurities of Ema are well known 3-valence electron ions, including boron (B).

6. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun '764 as applied to claim 7 above, and further in view of Mitani et al. (JP. Patent No. 10-223497).

With respect to claim 19, Sun teaches step c) including: pre-bonding the respective front faces of the first (20) and second (10) semiconductor wafer.

Thus, Sun is shown to teach all the features of the claim with the exception of disclosing the details of the process.

However, Mitani in bonding two semiconductor wafers teaches: arranging the first (2) and second (3) semiconductor wafers so that their respective front faces are adjacent each other; and vertically applying a force to a back face of a bonded surface of the first (2) and second (3) semiconductor wafers. (See Fig. 1D, [0021]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to pre-bonding the semiconductor wafer of Sun as taught by Mitani because this step is an obvious process step before the heat since the two semiconductor wafers must be contacting each other so that bonding can be effective.

With respect to claim 20, the bonding of Mitani further includes performing in the atmosphere containing water vapor, thus, the limitation of absorbing certain $H_2O$ vapor into the surfaces at which the first and second semiconductor wafers are bonded with each other is met.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anh D. Mai
August 17, 2004